Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor memory comprising:

a pair of diffused layers formed in a surface area of a semiconductor substrate; and

a gate electrode formed on a gate insulating film on the semiconductor substrate between said pair of diffused layers, so that carriers are trapped in the gate insulating film by applying a predetermined voltage to said gate electrode, thereby 2-bit information is capable of being recorded, and wherein

the gate insulating film is formed higher in carrier trap characteristic at positions near said pair of diffused layers than in a remaining area.

Claim 2 (Original): A semiconductor memory according to claim 1, wherein a charge trap film higher in carrier trap characteristic than said gate insulating film is formed in said gate insulating film at the positions near said pair of diffused layers.

Claim 3 (Original): A semiconductor memory according to claim 2, wherein said gate insulating film is formed thinner at the positions near said pair of diffused layers than in the remaining area.

Claim 4 (Original): A semiconductor memory according to claim 1, wherein said gate insulating film is formed smaller in film thickness in electrical capacitance conversion at the positions near said pair of diffused layers than in the remaining area.

Claim 5 (Original): A semiconductor memory according to claim 2, wherein another charge trap film is formed on said gate insulating film, and said gate electrode is formed on said other charge trap film on said gate insulating film.

Claim 6 (Withdrawn): A method of manufacture of a semiconductor memory, comprising:

a first step for sequentially forming first and second insulating films on a semiconductor substrate;

a second step for selectively removing and patterning said first and second insulating films;

a third step for forming a third insulating film on said semiconductor substrate in a predetermined range from said exposed semiconductor substrate to a layer below said second insulating film;

a fourth step for introducing impurities into said semiconductor substrate by utilizing said second insulating film as a mask, thereby forming a pair of independent diffused layers in a surface area of said semiconductor substrate at two sides of said second insulating film;

a fifth step for leaving said third insulating film formed in the predetermined range below said second insulating layer, and removing said third insulating film in a remaining area to expose

said semiconductor substrate;

a sixth step for thermally oxidizing said exposed semiconductor substrate to form an element isolation film;

a seventh step for removing said first and second insulating films to expose said underlying semiconductor substrate and third insulating film, and causing said third insulating film to function as a charge trap film;

a eighth step for thermally oxidizing the exposed surface of said semiconductor substrate to form a fourth insulating film, and covering upper and lower surfaces of said charge trap film with the fourth insulating film;

a ninth step for forming a conductive film on said fourth insulating film; and

a tenth step of patterning said conductive film into a gate electrode shape.

Claim 7 (Withdrawn): A method of manufacture of a semiconductor memory according to claim 6, further comprising, between said second and third steps, the eleventh step for removing said first insulating film by a predetermined amount in a direction of pattern width to make the pattern width of said first insulating film smaller than the pattern width of said second insulating film, and

wherein

in the third step, said third insulating film is formed on said exposed semiconductor substrate and on said semiconductor substrate within a range of said predetermined amount.

Claim 8 (Withdrawn): A method of manufacture of a semiconductor memory according to claim 6, further comprising, between said eighth and ninth steps, the twelfth step for forming a fifth insulating film on said fourth insulating film, and wherein

in the ninth step, said conductive film is formed on said fifth insulating film on said fourth insulating film.

Claim 9 (Withdrawn): A method of manufacture of a semiconductor memory, comprising the steps of:

forming a first insulating film on a semiconductor substrate;

selectively removing said first insulating film to expose said underlying semiconductor substrate;

introducing impurities into said exposed semiconductor substrate by using said first insulating film as a mask;

forming a pair of independent impurity diffused layers in a surface area of said semiconductor substrate at two sides of said first insulating film;

forming a second insulating film so as to cover said impurity diffused layers and said first

removing said second insulating film on said first insulating film to expose said first insulating film;

removing said first insulating film to expose said underlying semiconductor substrate, thereby

causing this area to function as an active element area;

forming a third insulating film on said semiconductor substrate in said active element area;

forming a fourth insulating film on said third insulating film;

forming a fifth insulating film so as to cover said fourth and second insulating films;

removing said fifth insulating film so as to remain only on two sides of said active element area, thereby forming a side wall of said fifth insulating film on a side wall of said second insulating film and exposing said semiconductor substrate in said active element area;

forming a sixth insulating film on said exposed semiconductor substrate;

removing said side wall to expose said underlying fourth insulating film of said side wall, thereby causing said fourth insulating film to function as a charge trap film;

forming a seventh insulating film on said charge trap film; and

forming a conductive film so as to cover said sixth and seventh insulating films.

Claim 10 (New): A semiconductor memory comprising:

a pair of diffused layers formed in a surface area of a semiconductor substrate; and

a gate electrode formed on a gate insulating film on the semiconductor substrate between said pair of diffused layers, so that carriers are trapped in the gate insulating film by applying a predetermined voltage to said gate electrode, and wherein

the gate insulating film is formed higher in carrier trap characteristic at positions near said pair of diffused layers than in a remaining area,

a charge trap film higher in carrier trap characteristic than said gate insulating film is formed in said gate insulating film at the positions near said pair of diffused layers, and

another charge trap film is formed on said gate insulating film, and said gate electrode is formed on said other charge trap film on said gate insulating film.

Amendments to the Drawings:

The attached sheet of drawings includes changes to Fig. 8. This sheet, which includes Fig.8, replaces the original sheet including Fig. 8. Amended Fig. 8 has been labeled as prior art as suggested by the Examiner on page 2 of the outstanding Office Action.